

**Open Networking Conference Japan 2020** 

### データプレーン高速化技術の最新アップデート

インテル株式会社 森 直之, 2020/10/15



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Intel technologies' features and benefits depend on system configuration and may require enabled hardware, software or service activation. Performance varies depending on system configuration.

Performance results are based on testing as of dates shown in configurations and may not reflect all publicly available updates. See backup for configuration details. No product or component can be absolutely secure.

Tests document performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. For more complete information about performance and benchmark results, visit http://www.intel.com/benchmarks.

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Hyper-Threading Technology requires a computer system with a processor supporting HT Technology and an HT Technology-enabled chipset, BIOS and operating system. Performance will vary depending on the specific hardware and software you use. For more information including details on which processors support HT Technology, see <u>here</u> Intel® Turbo Boost Technology Requires a system with Intel® Turbo Boost Technology. Intel® Turbo Boost Technology and Intel® Turbo Boost Technology 2.0 are only available on select Intel® processors. Consult your PC manufacturer. Performance varies depending on hardware, software, and system configuration. For more information, visit <u>http://www.intel.com/go/turbo</u>

No computer system can provide absolute security under all conditions. Intel<sup>®</sup> Trusted Execution Technology (Intel<sup>®</sup> TXT) requires a computer with Intel<sup>®</sup> Virtualization Technology, an Intel<sup>®</sup> TXT-enabled processor, chipset, BIOS, Authenticated Code Modules and an Intel<sup>®</sup> TXT-compatible measured launched environment (MLE). Intel<sup>®</sup> TXT also requires the system to contain a TPM v1.s. For more information, visit <u>http://www.intel.com/technology/security</u>

The original equipment manufacturer must provide TPM functionality, which requires a TPM-supported BIOS. TPM functionality must be initialized and may not be available in all countries.

Code names are used by Intel to identify products, technologies, or services that are in development and not publicly available. These are not "commercial" names and not intended to function as trademarks.

Roadmap not reflective of exact launch granularity and timing - please refer to ILU guidance

Intel<sup>®</sup> Virtualization Technology requires a computer system with an enabled Intel<sup>®</sup> processor, BIOS, virtual machine monitor (VMM). Functionality, performance or other benefits will vary depending on hardware and software configurations. Software applications may not be compatible with all operating systems. Consult your PC manufacturer. For more information, visit <u>http://www.intel.com/go/virtualization</u>

Intel<sup>®</sup> AES-NI requires a computer system with an AES-NI enabled processor, as well as non-Intel<sup>®</sup> software to execute the instructions in the correct sequence. AES-NI is available on select Intel<sup>®</sup> processors. For availability, consult your reseller or system manufacturer. For more information, see Intel<sup>®</sup> Advanced Encryption Standard Instructions (AES-NI)

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### Agenda

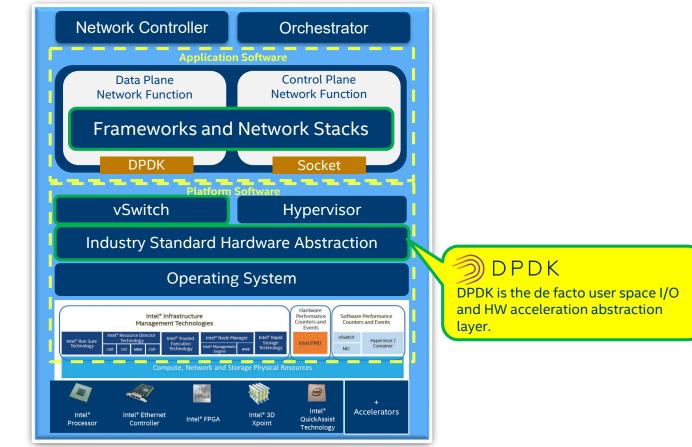
- DPDK\* Overview
- DPDK and AF\_XDP
- Intel<sup>®</sup> Ethernet Adaptors and processors
- DPDK Roadmap
- Intel<sup>®</sup> Scalable I/O Virtualization
- Further Information



# **DPDK OVERVIEW**



### Network Platform Framework (Data Plane View)





### **DPDK Components**

I security protocols

IGB\_UIO

KNI



#### **DPDK Fundamentals**

- Implements run-to-completion and pipeline models
- No scheduler all devices accessed by polling
- Supports 32-bit and 64-bit OSs, with and without NUMA
- Scales from Intel® Atom® to Intel® Xeon® processors
- Number of cores and processors is not limited
- Optimal packet allocation across DRAM channels
- Use of 2M & 1G hugepages and cache aligned structures
- Uses bulk concepts processing 'n' packets simultaneously
- Open source and BSD licensed

• Ease of Development - quick prototyping with samples, debugging (gdb), Analysis (VTune<sup>™</sup>, Intel<sup>®</sup> Performance Counter Monitor (Intel<sup>®</sup> PCM), PROX)

#### DPDK Applications - Network Functions (Cloud, Enterprise, Telco)

Core libraries	Packet classification	Accelerated SW libraries	Stats	QoS	Packet Framework
Core functions such as memory management, software rings, timers etc.	Software libraries for hash/exact match, LPM, ACL, etc.	Common functions such as fragmentation, reassembly, reordering etc.	Libraries for collecting and reporting statistics & metrics.	Libraries for QoS scheduling and metering/policing	Libraries for creatin complex pipelines i software.
ETHDEV	RAWDEV	CRYPTODEV		EVENTDEV	BBDEV
Flow API, MTR API, TM API PMDs for physical and virtual Ethernet devices	PMDs for raw devices	PMDs for HW and SW crypto accelerators	PMDs for HW and SW compression accelerators	Event-driven PMDs	PMDs for HW and SW wireless accelerators
devices	/	()	·/	i/	l
HW and SW acceleration of					

UIO\_PCI\_GENERIC

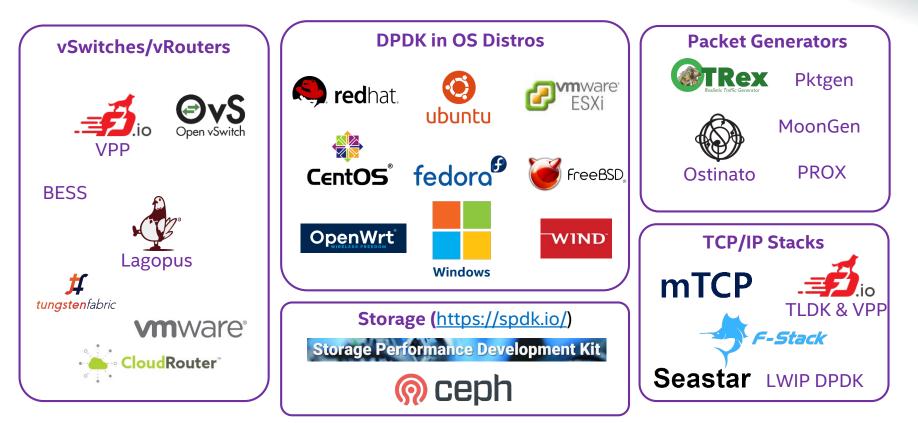
VFIO

Kernel

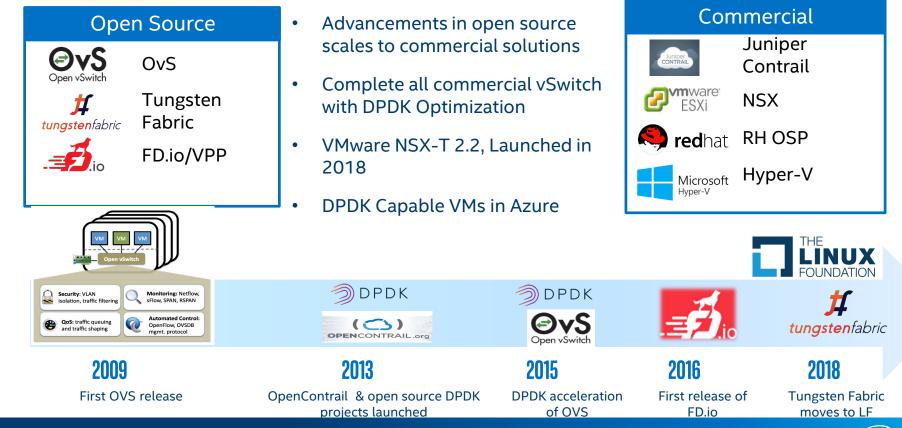
AF\_XDP

### **Projects Using DPDK**



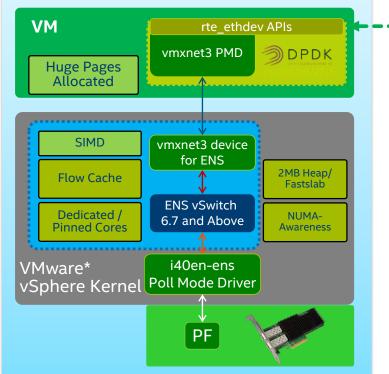


### Intel Virtual Switch Investment



### VMware vCloud Accelerated Performance

N-VDS Based on DPDK technology



Accelerate VNF ecosystem for more performance with DPDK APIs



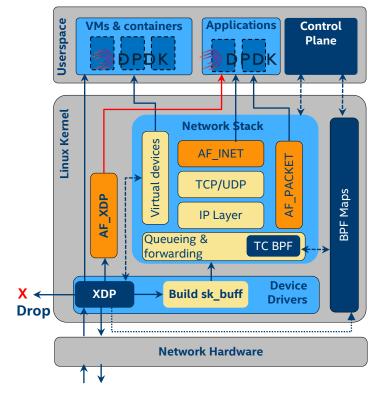




### **AF\_XDP** Overview

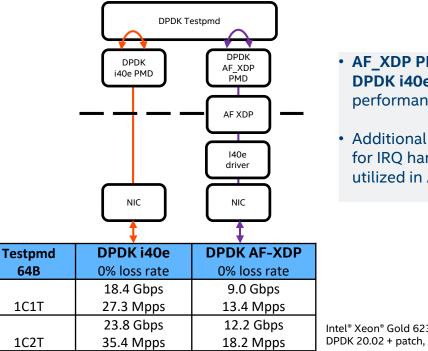
Packet movement between kernel and userspace

- New socket AF\_XDP is an address family for high performance packet processing in the kernel
- XDP (eXpress Data Path) can redirect frames to a memory buffer in userspace by eBPF (or route packets to Linux stack)
- DMA transfers use user space memory (zero copy between user space and kernel space)
- Connect XDP pass-through to user-space directly
- No change in DPDK apps, kernel driver handles hardware
- Maintains Linux properties (Security, isolation, robustness).
- Can be used with Drivers that support XDP
- Lots of new possible uses, other net drivers (Virtio, vEth)





### DPDK + AF\_XDP PMD Performance Summary



 AF\_XDP PMD is 50% of DPDK i40e PMD driver performance.

 Additional 2 cores (2C4T) for IRQ handling will be utilized in AF\_XDP

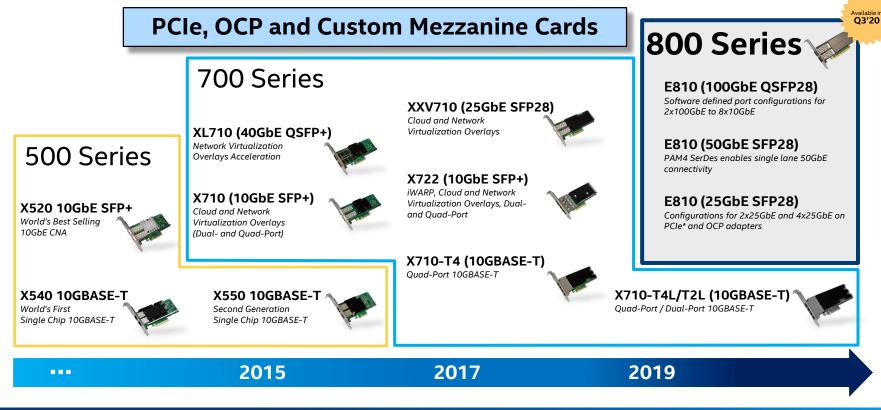
Intel® Xeon® Gold 6230 CPU @2.10GHz DPDK 20.02 + patch, Open vSwitch\* 2.13 , Ubuntu\*-19.04 (Kernel 5.4.25)

Disclaimer: Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <a href="http://www.intel.com/performance">http://www.intel.com/performance</a>. Source: Intel internal testing. Features & schedule are subject to change.

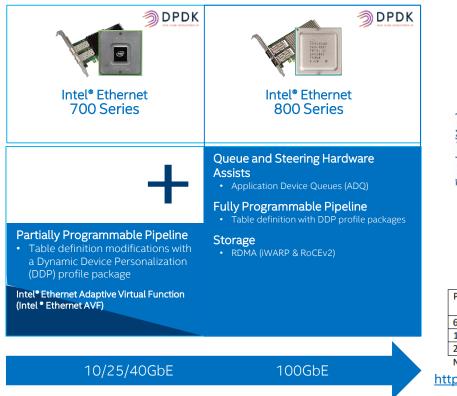
# **INTEL® ETHERNET ADAPTORS**



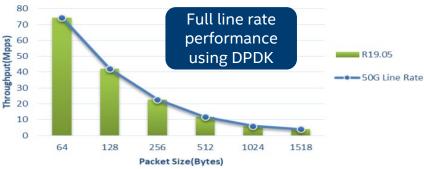
### Intel<sup>®</sup> Ethernet Adapter Roadmap Summary (10GbE and higher by series)



### Intel® Ethernet Architecture Enhanced with DPDK



DPDK L3fwd RFC2544 Zero Packet Loss Performance on 2x Intel(R) Ethernet Network Adapter XXV710-DA2(1port per NIC)



#### 4 logical cores, 4 queues for 2 ports

Packet Size (Bytes)	Throughput with 2c2t2q per port(Mpps)	Line rate%
64	74.4	100
128	42.22	100
256	22.64	100

Note: All packet sizes over 64B reach line rate.

http://fast.dpdk.org/doc/perf/DPDK 20 05 Intel NIC performance report.pdf

Features & schedule are subject to change. All products, computer systems, dates and figures specified are preliminary based on current expectations, and are subject to change without notice.

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### Changing Network Landscapes – Changes Protocol Needs

Significant expansion of protocol types that network adapters need to parse



Network Virtualization over Layer 3 (NVO3)

Virtual Extensible LAN (VXLAN) [RFC7348]

Generic Protocol Extension for VXLAN (VXLAN-GPE)

Network Virtualization using Generic Routing Encapsulation (NVGRE) [RFC7637]

Generic Network Virtualization Encapsulation (GENEVE)

Network Service Header (NSH)



C-VLAN Tag (C-Tag) Customer VLAN (C-VLAN) S-VLAN tag (S-Tag) Service VLAN (S-VLAN) Customized Protocols



### Network Edge

GPRS Tunneling Protocol (GTP) Internet Protocol over Ethernet (IPoE) Layer 2 Tunneling Protocol (L2TP) Multiprotocol Label Switching (MPLS) Multi-Service BNG (MS-BNG) Residential Gateway (RG) Point to Point Protocol (PPP) PPP over Ethernet (PPPoE) Control and Provisioning of Wireless Access Points (CAPWAP)

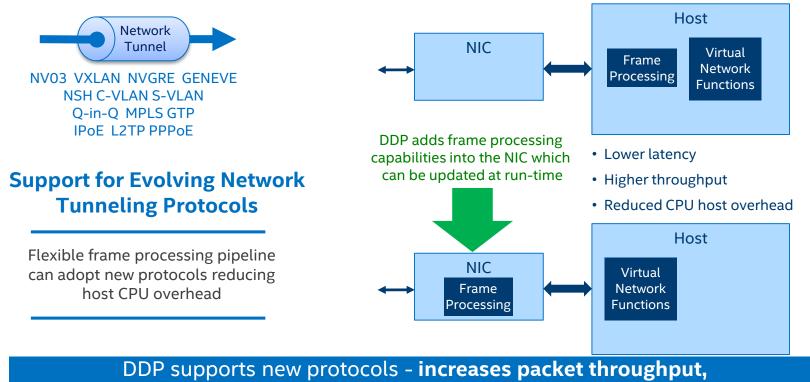


Internet Protocol Security (IPsec) Encapsulating Security Payloads (ESP) Authentication Headers (AH) Security Associations (SA)

(intel)

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### The Need for Dynamic Device Personalization (DDP)



reduces packet latency for Intel® Ethernet 700 Series and Intel® Ethernet 800 Series

### **Dynamic Device Personalization (DDP)**

#### **RUN-TIME PROGRAMMABILITY**

Packet pipeline customization to meet a wide range of customer deployment needs

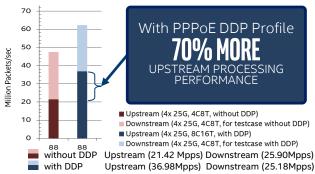
#### Available on Intel<sup>®</sup> Ethernet 700 Series

#### Unsupported protocols in the pipeline rely on the host to parse them

#### **OPTIMIZE PERFORMANCE**

- Lower Latency
- Higher Throughput
- Improved CPU Utilization

Improved Packet Processing Efficiency Broadband Remote Access Server (BRAS) Aggregated Forwarding Test



Dynamic Device Personalization (DDP) profile enabled

The pipeline parser can look deeper into the packets



your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit http://www.intel.com/performance.

Source: Intel internal testing as of November 2017. <sup>1</sup> Features & schedule are subject to change. Calculation: Upstream DDP vs w/o DDP ((36.98-21.42)/21.42\*100%) = 72.6%

(intel)

### Summary of Dynamic Device Personalization (DDP) When used with DPDK

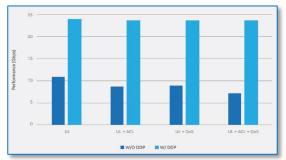
- Enables processing of new protocols using existing hardware
- Intel<sup>®</sup> Ethernet 700 and 800 Series
- Industry standard or custom profiles

### Intel provides a wide variety of 700 and 800 Series products

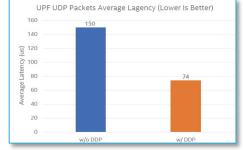
- 10GbE, 25GbE, 40GbE, 100GbE
- PCI-Express\* or OCP\* form factors
- Single, dual or quad ports

### Improves network performance while reducing CPU utilization

- · Improves packet per second processing rates
- Reduces processing latency and latency variation
- Reduces CPU utilization



#### 2-3x throughput improvement in vBNG test case<sup>1</sup>



#### 2x latency reduction with TCP in GTP-U traffic test case<sup>2</sup>

Disclaimer: Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <a href="http://www.intel.com/performance">http://www.intel.com/performance</a>.
<sup>1</sup>Data from Intel-NetElastic <a href="http://www.intel.com/performance">white paper</a>



### Intel<sup>®</sup> Ethernet Controller E810

#### General Purpose Ethernet Controller with Programmable Pipeline for broad deployment

#### Features

#### Three SKUs:

- E810-CAM2(100Gb throughput):25x25mm; PCI Express\* 4.0/3.0 x16/x8; 2x100Gb, 8x10Gb, and more
- E810-CAM1(100Gb throughput):25x25mm; PCI Express\* 4.0/3.0 x16/x8; 1x100Gb, and more
- E810-XXVAM2(50Gb throughput):21x21mm; PCI Express\* 4.0/3.0 x8; 1x50Gb, 2x25Gb, and more

#### NFV and Network Virtualization Overlay (NVO) Support

- Dynamic Device Personalization (DDP) with fully programmable pipeline for flexible frame format support
- Intelligent Flow Direction: Receiver Side Scaling (RSS), Intel<sup>®</sup> Ethernet Flow Director, Application Device queues (ADQ)
- Comprehensive Network Virtualization Overlay protocols Support
- vSwitch Assist
- QoS: Priority-based Flow Control(802.1Qbb); Enhanced Transmission Selection(802.1Qaz); Differentiated Services Code Point (DSCP)

#### Server Virtualization Support

- SR-IOV: 8PFs, 256VFs, 256 Queues per PF, 2k queue pairs total, 768 VSIs;
- Adaptive VF driver;
- Programmable Virtual Ethernet Bridging (VEB) with ACL;
- Virtual Machine Device Queue (VMDq); Virtual Machine QoS (VMQoS)

#### **Remote Direct Memory Access (RDMA)**

Both iWARP and RoCEv2 support selectable via software per port

#### Storage Networking

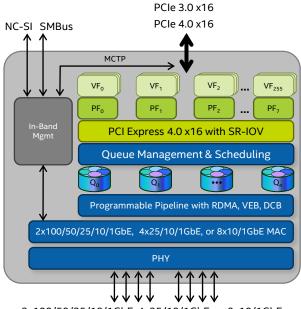
- Data Center Bridging (DCB);
- Stateless L3/L4 offloads for iSCSI, NAS, NFS;
- Server Message Block (SMB)

#### **Precision Clocks Synchronization**

IEEE 1588 PTP/802.1AS

#### Management

- NC-SI 1.1, MCTP over SMBus, MCTP over PCIe, OS2BMC;
- PXE boot support and EFI based iSCSI boot; WoL (Wake On LAN);



2x100/50/25/10/1GbE, 4x25/10/1GbE, or 8x10/1GbE





# INTEL<sup>®</sup> XEON<sup>®</sup> PROCESSOR SCALABLE FAMILY NFV SKU



Intel Networking/NFV Specialized SKUs - 5218N, 6230N and 6252N



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VNF 2

VNF 1

CPU

Incremental ~10% Performance Increase (2.3GHz vs 2.1GHz)<sup>1</sup> without any code changes on NFV workloads for 6230N & 6252N



Dynamic configuration of CPU Frequency Boost Performance for target NFV Workload at Runtime

<sup>1</sup>Exclude 5218N, 5218N provides Thermal Design Specification at 110W over 5218 at 125W <sup>2</sup>Please contact your vendor for product support details

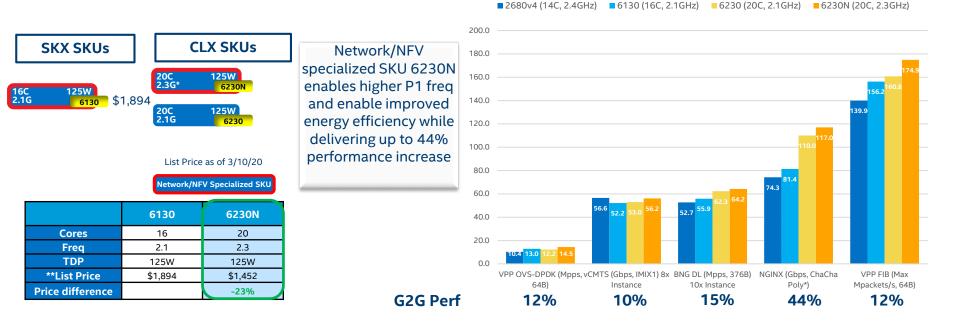
CLX 6252N (24C@2.3ghz @ 150W) vLB and vSW are running **High Priority** Standard Priority Hi Priority Frequency Performance increase vLB vSW Base Frec Base Freg Cores Cores ค without code modificatio 2.8 (GHz) 16 2.1(GHz) High Priority Cores CLX 6230N (20C@2.3ghz@125W) 27GHz vRTR vFW Standard Priority High Priority vRTR and vFW are non mission critical Base Freq Cores Base Freq Cores running Standard Frequency at 2.1GHz 2.7 (GHz) 14 2.1(GHz) Standard Priority Cores 2 1GHz CLX 5218N (16C@2.3ghz@ 110W) **High Priority** Standard Priority Performance Boost for VNF Base Freq Cores Base Fred Cores 12 2.1 (GHz) 2.7 (GHz)

Intel<sup>®</sup> Speed Select Technology – Base Frequency

Performance results are based on testing Intel as of 2/4/2019 and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure. Software and workloads used in performance tests may have been optimized for performance only on Intel microprocessors. Performance tests, such as SYSmark and MobileMark, are measured using

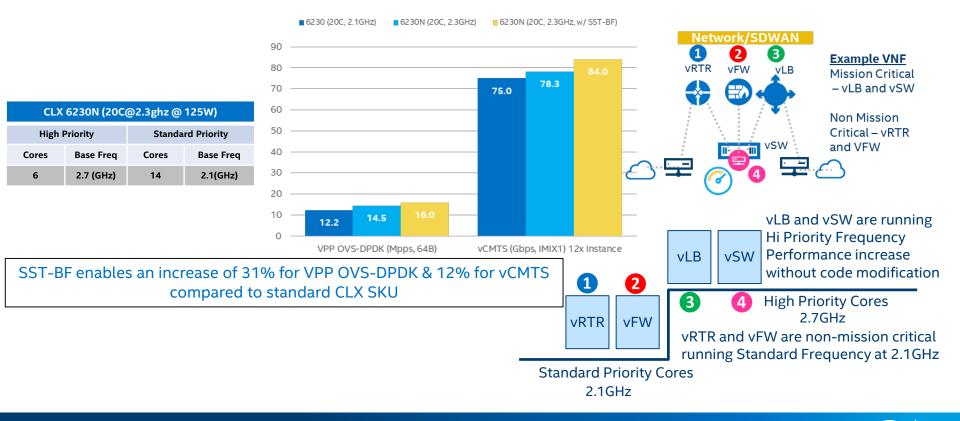
specific computer systems, components, software, operations and functions. Any change to any of those factors may cause the results to vary. You should consult other information and performance tests to assist you in fully evaluating your contemplated purchases, including the performance of that product when combined with other products. For more complete information visit <u>www.intel.com/benchmarks</u>.

### ~10% PERF INCREASE (2.3GHZ VS 2.1GHZ) WITHOUT ANY CODE CHANGES (6230N vs. 6230)



Performance results are based on testing by Intel as of 8/8/2019 and may not reflect all publicly available security updates. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. See configuration slide for details. For optimization, please visit https://software.intel.com/en-us/articles/optimization-notice. \*ECDHE-RSA2K CHACHA20-POLY1305

### 2 DYNAMIC CONFIG OF CPU FREQUENCY DELIVERS MORE PERFORMANCE FOR NFV



Performance results are based on testing by Intel as of 8/8/2019 and may not reflect all publicly available security updates. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks. See configuration slide for details. For optimization, please visit https://software.intel.com/en-us/articles/optimization-notice.

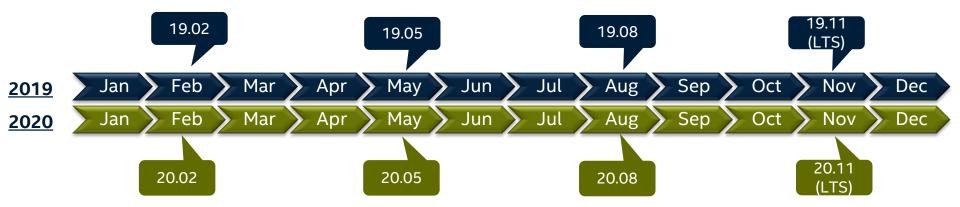
# **DPDK ROADMAP**





### 2019 & 2020 Releases

Using Ubuntu\* numbering scheme of YY.MM as of 16.04



DPDK Long-Term Support (LTS) provides a stable release maintained for 2 years with back-ported bug fixes. Provides a stable target on which to base applications or packages.

- Bug fixes that do not change the ABI will be back-ported.
- In general, new features will not be back-ported. There may be occasional exceptions where the following criteria are met:
  - There is a justifiable use case (for example a new PMD).
  - The change is non-invasive.
  - The work of preparing the back-port is done by the proposer.
  - There is support within the community.



### **DPDK Roadmap Priorities**

#### New Hardware Support

- CPUs, standard NICs, smart NICs, look-aside and inline accelerators, coherent FPGAs, programmable accelerator cards etc.
- DPDK FPGA reference layer

#### Hardware Abstraction (Acceleration APIs)

- Completion of compression
- Intel QAT acceleration for asymmetric crypto
- Hardware acceleration for eventdev (HQM) and bbdev

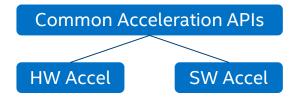
#### Power Management

- Provide intelligence to match power consumption to processing load
- Expose CPU power management features through DPDK









### **DPDK Roadmap Priorities**



Unstream



#### **Cloud Friendly Features**

- Dynamic memory allocation
- Improved sharing of I/O resources. Improved usability/configurability

#### Next-Generation Central Office (NGCO)

- Functional improvements and performance optimizations to support NGCO initiative
- Broadband Remote Access Server (BRAS) Press Press Broadband Remote Access Server (BRAS) Press P





#### Security Protocol Acceleration

- Native DPDK IPsec library to support hardware and software acceleration
- Optimized SA/SP database look-up to improve scalability

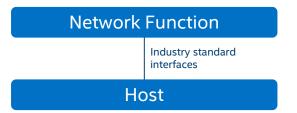


### **DPDK Roadmap Priorities**



#### **Network Function (VNF/CNF) Abstraction**

- Continued enhancements to vhost-virtio (performance improvements, virtio 1.1, mdev, memif, hotplug/live migration etc.)
- Intel<sup>®</sup> Ethernet Adaptive Virtual Function software back-end to support vswitch and live migration





#### **Broad Market**

Support for DPDK on Windows, Azure, VMware

#### Notes:

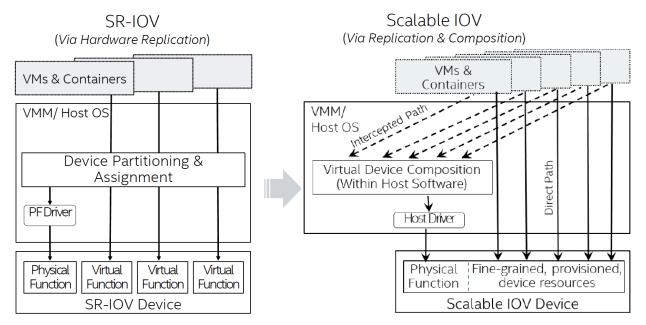
- 1. Items listed in this slide and the previous two slides are not in priority order.
- 2. Roadmap is subject to change without prior notice.

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# INTEL<sup>®</sup> SCALABLE I/O VIRTUALIZATION



### SR-IOV $\succeq$ Intel<sup>®</sup> Scalable IOV



Intel<sup>®</sup> Scalable I/O Virtualization Technical Specification

Sep 2020, Reference Number: 337679-002, Revision: 1.1 and Jun 2018, Reference Number: 337679-001, Revision: 1.0 https://software.intel.com/sites/default/files/managed/cc/0e/intel-scalable-io-virtualization-technical-specification.pdf

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# **FURTHER INFORMATION**



 Plan on attending a future Summit to get involved and make connections. Find out about events at <u>https://www.dpdk.org/events/</u>

 Check out the great video content from the years full of useful information and ideas of new concepts and how to get better performance. All sessions will be recorded and available on the <u>DPDK YouTube Channel</u> after the events

#### Summits from the years & different locations

DPDK userspace Summit Updated today	DPDK 25 Opening Remarke = 2019 DPDK Summit North America	DPDK Userspace, Bordeaux 2019 View Full PLAYLIST	DPDK 15 5 5 2019 DPDK China VIEW FULL PLAYLIST	2019 DPDK India VIEW FULL PLAYLIST	2018 DPDK San Jose View Full PLAYLIST
VIEW FULL PLAYLIST	VIEW FULL PLAYLIST		44 =,	DPDK DPDK on Embedded N 23 SoCa - Expansional & N	7 ₽,
2018 DPDK PRC Summit China VIEW FULL PLAYLIST	2018 DPDK Userspace, Dublin VIEW FULL PLAYLIST	2018 DPDK Summit India VIEW FULL PLAYLIST	2017 DPDK Summit USA VIEW FULL PLAYLIST	2016 DPDK Summit USA VIEW FULL PLAYLIST	2015 DPDK Summit San Francisco VIEW FULL PLAYLIST
2016 DPDK Summit China/Asia	23 2017 Userspace Dublin	2017 DPDK Summit India	24 = 2016 Userspace Dublin	2015 Userspace Dublin	

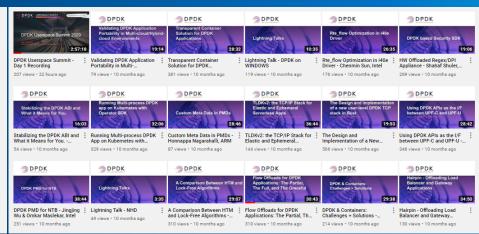
Pacific

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#### 2020 Topics

Story of perfect system tuning for latency measurement DPDK for ultra low latency applications Do DPDK APIs provide the highest performance? Introducing flow performance application Debugging DPDK applications using rr eBPF Probes in DPDK applications for troubleshooting and monitoring Cheat sheet to migrate from GNU make to meson Stateful Flow Table (SFT) - Connection tracking in DPDK Device virtualization in DPDK vDPA: on the road to production Key take aways from QUIC acceleration with DPDK Accelerating O-RAN fronthaul with DPDK

#### Video's from all the summits available



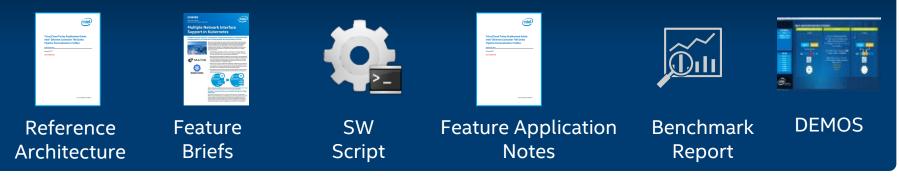
**USERSPACE SUMMIT** 

SEPTEMBER 22-23, 2020 • VIRTUAL EXPERIENCE

### WHAT ARE EXPERIENCE KITS?

Deliver Network Transformation Experience Kits to ease capability **consumption** in commercial deployments

#### A LIBRARY OF BEST PRACTICE DEVELOPMENT GUIDELINES THAT SHOW AND TELL...



Check the Network Transformation Experience Kits on Intel Network Builder: <u>https://networkbuilders.intel.com/network-technologies/network-transformation-exp-kits</u>

## **OPTIMIZATION NOTICE**

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